Amended Pages under Art. 34
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CLAIMS

1. (amended) A semiconductor device comprising a MIS type field effect transistor, wherein the transistor comprising:

a silicon substrate;

a gate insulating film comprising a high-dielectric-constant metal oxide film and a silicon containing insulating film lying between the metal oxide film and the silicon substrate;

a silicon containing gate electrode formed on the gate insulating film; and

a sidewall including silicon oxide as a constituting material, which is formed on each lateral face side of the gate electrode; and

wherein a silicon nitride film is interposed between the sidewall and at least the lateral face of the gate electrode, and

wherein the silicon nitride film covers the lateral face of the high-dielectric-constant metal oxide film, and a silicon oxide film underlies the silicon nitride film.

2. (amended) The semiconductor device comprising the MIS type field effect transistor according to Claim 1, wherein the silicon nitride film is laid between the sidewall and the silicon substrate.

3. (amended) The semiconductor device comprising the MIS type field effect transistor according to Claim 1, wherein the silicon nitride film is absent between the sidewall and the silicon substrate.

4. A semiconductor device comprising a MIS type field effect transistor, wherein the transistor comprising:

a silicon substrate;

a gate insulating film comprising a high-dielectric-constant metal oxide film and a silicon containing insulating film lying between the metal oxide film and the silicon substrate; and

a silicon containing gate electrode formed on the gate insulating film; and

wherein the high-dielectric-constant metal oxide film has a nitrogen containing section at least on each of its lateral face sides.

5. The semiconductor device according to Claim 4, wherein the nitrogen-containing section is a silicon nitride film covering at least the lateral face of the high-dielectric-constant metal oxide film.

6. The semiconductor device according to Claim 5, wherein each lateral face of the gate insulating film has a recess with respect to the plane of the lateral face of the gate electrode, and, inside the recess, the silicon nitride film covers at least the lateral face of the high-dielectric-constant metal oxide film.

7. The semiconductor device according to Claim 4, wherein the nitrogen containing section is formed by applying a nitriding treatment to each lateral face section of the high-dielectric-constant metal oxide film.

8. The semiconductor device according to any one of Claims 4 to

7, further comprising a sidewall including silicon oxide as a constituting material, which is formed on each lateral face side of the gate electrode.

9. The semiconductor device according to any one of Claims 1 to 8, wherein a silicon nitride film is laid between the high-dielectric-constant metal oxide film and the gate electrode.

10. The semiconductor device according to any one of Claims 1 to 9, wherein the high-dielectric-constant metal oxide film contains hafnium (Hf).

11. The semiconductor device according to any one of Claims 1 to 10, wherein a dielectric constant of the high-dielectric-constant metal oxide film is not less than 10.

12. The semiconductor device according to any one of Claims 1 to 3 and 8, wherein the high-dielectric-constant metal oxide film is absent beneath the sidewall.

13. The semiconductor device according to any one of Claims 1 to 12, wherein a gate length of the gate electrode is not greater than 1 μ m.

14 (canceled)

15 (canceled)

16. A method of manufacturing a semiconductor device comprising

the steps of:

forming a high-dielectric-constant metal oxide film over a silicon substrate after forming a silicon containing insulating film;

forming a film of a silicon containing gate electrode material over the high-dielectric-constant metal oxide film;

forming a gate electrode by patterning the film of a gate electrode material;

forming a pattern of the high-dielectric-constant metal oxide film and the silicon containing insulating film under the gate electrode by patterning the high-dielectric-constant metal oxide film and the silicon containing insulating film;

forming a first silicon oxide film over the entire surface at a temperature of not higher than 600 ℃;

forming a silicon nitride film on the first silicon oxide film;

forming a second silicon oxide film on the silicon nitride film; and

etching back the second silicon oxide film, the silicon nitride film and the first silicon oxide film and thereby forming a sidewall on each lateral face of the gate electrode with the first silicon oxide film and the silicon nitride film lying therebetween.

17. The method of manufacturing a semiconductor device according to Claim 16, further comprising, after the step of forming the silicon nitride film, the step of applying etch back to the silicon nitride film and the first silicon oxide film so that the silicon nitride film and the silicon oxide film lying on the gate electrode and the silicon substrate can be removed,

following which the second silicon oxide film is formed over the entire surface and by etching back the second silicon oxide film, a sidewall is formed on each lateral face of the gate electrode.

18. A method of manufacturing a semiconductor device comprising the steps of:

forming a high-dielectric-constant metal oxide film over a silicon substrate after forming a silicon containing insulating film;

forming a film of a silicon containing gate electrode material over the high-dielectric-constant metal oxide film;

forming a gate electrode by patterning the film of a gate electrode material;

forming a pattern of the high-dielectric-constant metal oxide film under the gate electrode by patterning the high-dielectric-constant metal oxide film;

removing at least each lateral face section of the pattern of the high-dielectric-constant metal oxide film by means of isotropic etching to form a recess;

forming a silicon nitride film over the entire surface so as to fill up the recess;

etching the silicon nitride film in such a way that, inside the recess, at least the silicon nitride film covering each lateral face of the high-dielectric-constant metal oxide film can remain; and

forming a silicon oxide film over the entire surface and then etching back the silicon oxide film, and thereby forming a sidewall on each lateral face of the gate electrode.

19. A method of manufacturing a semiconductor device comprising the steps of:

forming a high-dielectric-constant metal oxide film over a silicon substrate after forming a silicon containing insulating film;

forming a film of a silicon containing gate electrode material over the high-dielectric-constant metal oxide film;

forming a gate electrode by patterning the film of a gate electrode material;

forming a pattern of the high-dielectric-constant metal oxide film under the gate electrode by patterning the high-dielectric-constant metal oxide film;

applying a nitriding treatment to each lateral face section of the pattern of the high-dielectric-constant metal oxide film; and

forming a silicon oxide film over the entire surface and then etching back the silicon oxide film, and thereby forming a sidewall on each lateral face of the gate electrode.

20. A method of manufacturing a semiconductor device comprising the steps of:

forming a high-dielectric-constant metal oxide film over a silicon substrate after forming a silicon containing insulating film;

forming a film of a silicon containing gate electrode material over the high-dielectric-constant metal oxide film;

forming a gate electrode by patterning the film of a gate electrode material;

forming a pattern of the high-dielectric-constant metal oxide film under the gate electrode by patterning the high-dielectric-constant metal oxide film;

forming a silicon oxide film over the entire surface at a temperature of not higher than 600 ℃; and

etching back the silicon oxide film, and thereby forming a sidewall on each lateral face of the gate electrode.

21. (amended) The method of manufacturing a semiconductor device according to any one of Claims 18 to 20, wherein a pattern of the silicon containing insulating film is further formed under the gate electrode by patterning the silicon containing insulating film.

22. (amended) The method of manufacturing a semiconductor device according to any one of Claims 16 to 21, wherein the high-dielectric-constant metal oxide film contains hafnium (Hf).

23. (amended) The method of manufacturing a semiconductor device according to any one of Claims 16 to 22, wherein a dielectric constant of the high-dielectric-constant metal oxide film is not less than 10.

24. (amended) The method of manufacturing a semiconductor device according to any one of Claims 16 to 23, wherein a gate length of the gate electrode is not greater than 1 μ m.

25. (new) The semiconductor device according to Claim 1, 2 or

3, wherein a thickness of the silicon oxide film is within a range of 1 to 20 nm.

26. (new) The semiconductor device according to Claim 1, 2 or 3, wherein a thickness of the silicon oxide film is within a range of 5 to 10 nm.

27. (new) The semiconductor device according to Claim 1, 2 or 3, wherein a thickness of the silicon nitride film is within a range of 1 to 10 nm.

28. (new) The semiconductor device according to Claim 1, 2 or 3, wherein the high-dielectric-constant metal oxide film has a nitridation region on each of its lateral face sides.

29. (new) The semiconductor device according to Claim 1, 2 or 3, wherein the nitridation region is formed within a range of 1 to 20 nm in the direction from it's lateral face to inside of the gate electrode, and a nitrogen content in the region is not less than 5 %.

30. (new) The semiconductor device according to Claim 1, 2 or 3, wherein the nitridation region is formed within a range of 1 to 20 nm in the direction from it's lateral face to inside of the gate electrode, and a nitrogen content in the region is not less than 10 %.

31. (new) The method of manufacturing a semiconductor device according to Claim 16 or 17, wherein a temperature for forming the first silicon oxide film is within a range of 200 to 600 ℃.

32. (new) The method of manufacturing a semiconductor device according to Claim 16 or 17, wherein a temperature for forming the first silicon oxide film is within a range of 400 to 600 ℃.